Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Amended) A computer system comprising:

a memory system where at least some of the memory is designated as shared memory;

a transaction-based bus mechanism coupled to the memory system wherein the transaction-based bus mechanism includes a cache coherency transaction defined within its transaction set;

a single processor having a cache memory, the processor coupled to the memory system through the transaction based bus mechanism;

a plurality of system components coupled to the transaction-based bus mechanism;

a first request issued by one of the plurality of system components and addressed to the processor, wherein the first request indicates a request to perform a cache coherency operation; and

wherein the processor is configured to respond to the first request by treating the first request as an explicit command to perform the cache coherency operation.

2. (Original) The computer system of claim 1 wherein the first request is implemented independent of any interrupt mechanism in the processor.

3. (Original) The computer system of claim 1 wherein the processor response to the first request comprises executing the cache coherency operation without the assistance of instructions executed on the processor.

4. (Original) The computer system of claim 1 wherein the processor is further configured to respond to the first request by generating a response message

addressed to the system component that initiated the first request indicating status of the cache coherency operation.

5. (Original) The computer system of claim 1 wherein the cache coherency transaction comprises a cache flush transaction and the first request includes an address in the shared memory to be flushed from the cache.

6. (Original) The computer system of claim 5 wherein the processor is configured to respond to the first request by:

looking up the address in the cache;

when the lookup yields a miss, or a hit to a cache line that is unmodified with regard to main memory, the processor issues a response to the first request immediately;

when the lookup yields a hit to a cache line that is modified with regard to main memory, the processor causes a writeback of the specified line to main memory followed by a response to the first request addressed to the system component that generated the request.

7. (Original) The computer system of claim 1 wherein the cache coherency transaction comprises a cache purge transaction and the first request includes an address in the shared memory to be purged from the cache.

8. (Original) The computer system of claim 7 wherein the processor is configured to respond to the first request by:

looking up the address in the cache;

when the lookup yields a miss the processor issues a response to the first request;

when the lookup yields a hit to a cache line that is modified with regard to main memory, the processor causes a writeback of the specified line to main

memory followed by an invalidation of the cache line and a response to the first request addressed to the system component that generated the request; and when the lookup yields a hit to a cache line that is not modified with regard to main memory, the processor causes an invalidation of the cache line and a response to the first request addressed to the system component that generated the request.

9. (Amended) A method for managing cache coherency in a shared memory system having a plurality of modules, including a single processing unit, coupled to a system bus, the method comprising the steps of:

initiating a cache coherency transaction on the system bus using one of the plurality of modules; and

in response to the cache coherency transaction, causing the processing unit to execute a cache coherency operation.

10. (Original) The method of claim 9 wherein the step of initiating is performed without using an interrupt mechanism of the processing unit.

11. (Original) The method of claim 9 wherein the step of causing the processing unit to execute the cache coherency operation is performed without executing instructions on the processing unit.

12. (Original) The method of claim 9 further comprising: generating a response to the initiated cache coherency transaction using the processing module, wherein the response is addressed to the module that initiated the cache coherency transaction and the response indicates the cache state.

13. (Original) The method of claim 9 wherein the cache coherency transaction comprises a cache flush transaction and the step of initiating includes indicating an address in the shared memory to be flushed from the cache.

14. (Original) The method of claim 13 wherein the step of executing further comprises:

looking up the address in the cache;

when the lookup yields a miss, or a hit to a cache line that is unmodified with regard to main memory, issuing a response to the first request immediately;

when the lookup yields a hit to a cache line that is modified with regard to main memory, causing a writeback of the specified line to main memory followed by generating a response to the initiated transaction, wherein the response is addressed to the system component that generated the request.

15. (Original) The method of claim 9 wherein the cache coherency transaction comprises a cache purge transaction and the step of initiating includes indicating an address in the shared memory to be purged from the cache.

16. (Original) The method of claim 15 wherein the step of executing further comprises:

looking up the address in the cache;

when the lookup yields a miss issuing a response to the system component that initiated the transaction;

when the lookup yields a hit to a cache line that is modified with regard to main memory, casing a writeback of the specified line to main memory followed by an invalidation of the cache line and issuing a response addressed to the system component that initiated the transaction; and

when the lookup yields a hit to a cache line that is not modified with regard to main memory, invalidating the cache line followed by issuing a response addressed to the system component that initiated the transaction.